SN74LVT125-EP
3.3-V ABT QUADRUPLE BUS BUFFER WITH 3-STATE OUTPUTS

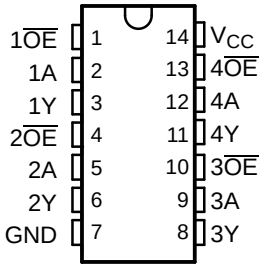
SCBS796A – JANUARY 2004 – REVISED JUNE 2005

FEATURES

- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Extended Temperature Performance of –40°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree(1)**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

D OR PW PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

This bus buffer is designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The SN74LVT125 features independent line drivers with 3-state outputs. Each output is in the high-impedance state when the associated output-enable ($\overline{OE}$) input is high.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

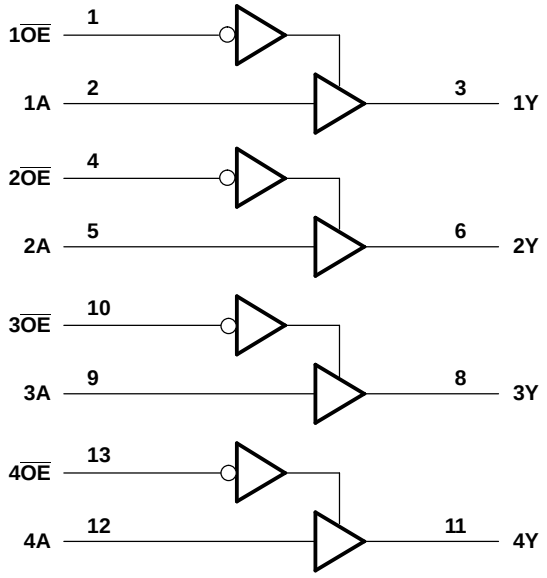
T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC – D	Tape and reel	SN74LVT125QDREP	LVT125E
	TSSOP – PW	Tape and reel	SN74LVT125QPWREP	LVT125E

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (EACH BUFFER)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	4.6	V
V_I	Input voltage range(2)		–0.5	7	V
V_O	Voltage range applied to any output in the high or power-off state(2)		–0.5	7	V
I_O	Current into any output in the low state			128	mA
I_O	Current into any output in the high state(3)			64	mA
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
θ_{JA}	Package thermal impedance(4)	D package		86	°C/W
		PW package		113	
T_{stg}	Storage temperature range(5)		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) This current flows only when the output is in the high state and $V_O > V_{CC}$.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.
(5) Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See http://www.ti.com/ep_quality for additional information on enhanced plastic packaging.

Recommended Operating Conditions(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage			5.5	V
I_{OH}	High-level output current			–32	mA
I_{OL}	Low-level output current			32	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	ns/V
T_A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA				–1.2	V
V_{OH}	V_{CC} = MIN to MAX(2),	I_{OH} = –100 µA		V_{CC} – 0.2			V
	V_{CC} = 2.7 V,	I_{OH} = –8 mA		2.4			
	V_{CC} = 3 V,	I_{OH} = –32 mA		2			
V_{OL}	V_{CC} = 2.7 V	I_{OL} = 100 µA				0.2	V
		I_{OL} = 24 mA				0.5	
	V_{CC} = 3 V	I_{OL} = 16 mA				0.4	
		I_{OL} = 32 mA				0.5	
I_I	V_{CC} = 0 or MAX(2),	V_I = 5.5 V				40	µA
	V_{CC} = 3.6 V	V_I = V_{CC} or GND	Control inputs			±1	
		V_I = V_{CC}	Data inputs			1	
		V_I = 0				–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V				±450	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	Data inputs	75			µA
		V_I = 2 V		–75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				5	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				–5	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND, I_O = 0		Outputs high		0.12	0.35	mA
			Outputs low		4.5	7	
			Outputs disabled		0.12	0.4	
ΔI_{CC}(3)	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6, Other inputs at V_{CC} or GND					0.2	mA
C_i	V_I = 3 V or 0				4		pF
C_o	V_O = 3 V or 0				8		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
(3) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

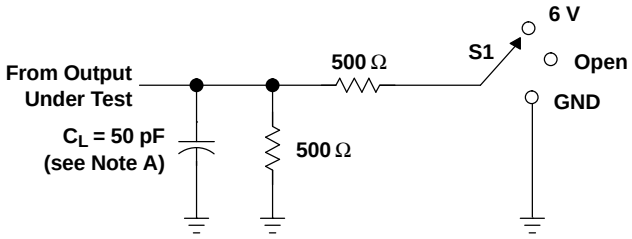
Switching Characteristics

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		UNIT
			MIN	TYP(1)	MAX	MIN	MAX	
t_{PLH}	A	Y	1	2.7	4.2		4.7	ns
t_{PHL}			1	2.9	4.1		5.1	
t_{PZH}	$\overline{OE}$	Y	1	3.4	4.9		6.2	ns
t_{PZL}			1.1	3.4	4.9		6.7	
t_{PHZ}	$\overline{OE}$	Y	1.8	3.7	5.3		5.9	ns
t_{PLZ}			1.3	2.6	4.7		4.2	

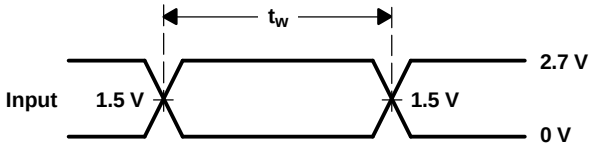
(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

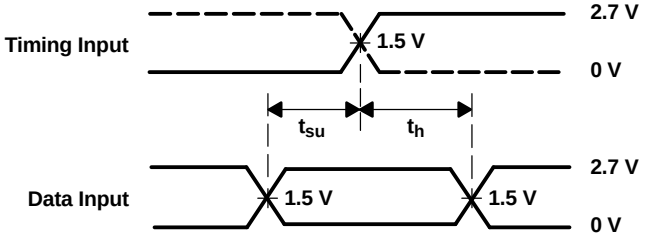


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

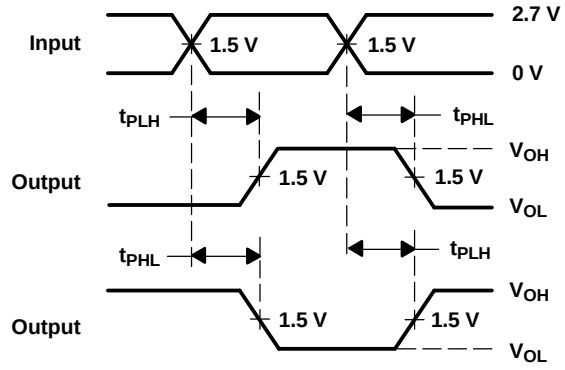
LOAD CIRCUIT FOR OUTPUTS



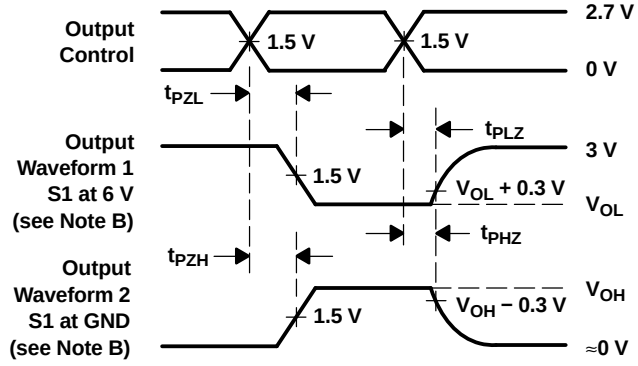
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN74LVT125QPWREP	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/04705-01XE	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

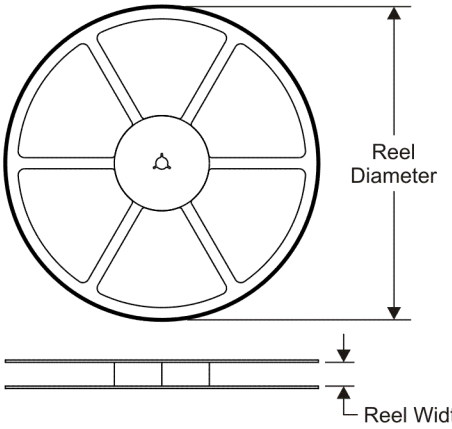
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

OTHER QUALIFIED VERSIONS OF SN74LVT125-EP :
- Catalog: SN74LVT125
- Automotive: SN74LVT125-Q1

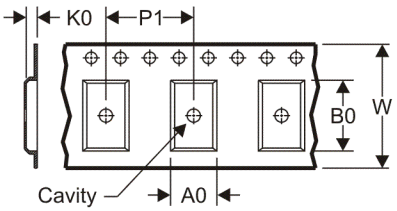
NOTE: Qualified Version Definitions:
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

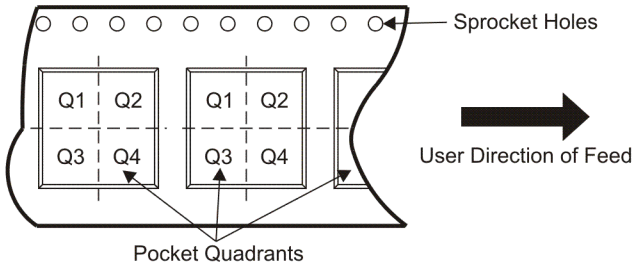


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

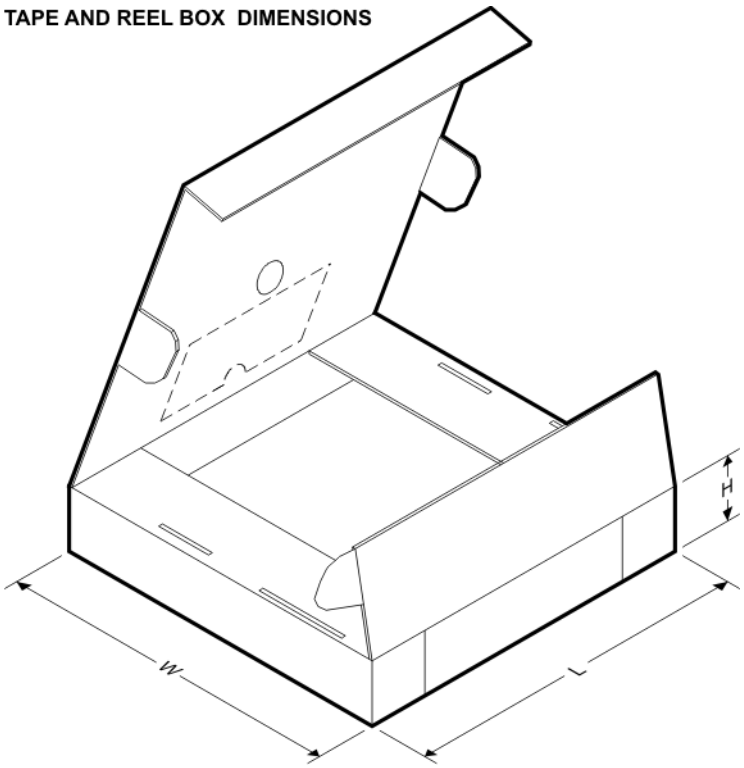
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVT125QPWREP	TSSOP	PW	14	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

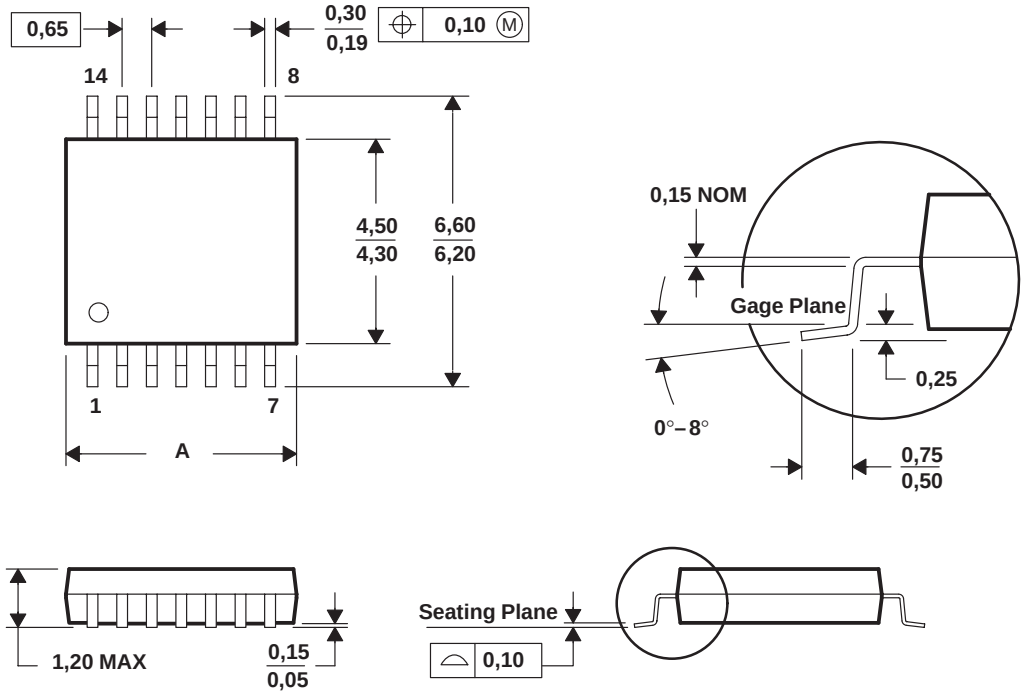


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVT125QPWREP	TSSOP	PW	14	2000	346.0	346.0	29.0

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

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NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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